WHAT IS CLAIMED IS:

1. A method for storing a result of a tuning process, comprising:

generating a first characteristic signal;

generating a second characteristic signal in response to a current signal;

determining an adjustment to the current signal based at least in part upon the first and second characteristic signals; and

storing a digital value representing the adjustment.

2. The method of Claim 1, further comprising:

repeating the steps iteratively; and

updating the digital value after each iteration.

3. The method of Claim 2, wherein:

the digital value comprises a plurality of bits; and

the method further comprises storing the result of each iteration in a bit of the digital value.

4. The method of Claim 2, further comprising:

counting the number of iterations; and

stopping the iterative repetition upon performing a predetermined number of iterations.

5. The method of Claim 2, wherein the adjustment to the current signal during a particular iteration is based on the last bit of the digital value stored.

6. The method of Claim 1, wherein the first characteristic signal comprises a voltage measured across a reference capacitor of a signal generator and the second characteristic signal comprises a voltage measured across a capacitor of a master circuit.

7. The method of Claim 6, wherein determining comprises comparing voltages across the respective capacitors when the reference capacitor reaches a predetermined voltage.

8. The method of Claim 1, wherein:

the second characteristic signal is generated using a master circuit that is part of an integrated circuit; and

the first characteristic signal is generated by a signal generator that comprises:

an external reference capacitor; and

an external reference resistor.

9. The method of Claim 1, wherein storing the digital value is performed even if circuitry used to complete the filter tuning process is powered down or disabled.

10. The method of Claim 1, wherein the step of determining comprises:

generating a clock signal when the first characteristic signal reaches a predetermined voltage;

storing a data signal in response to the clock signal, the data signal indicating whether the second characteristic signal is greater than or less than the first characteristic signal.

11. The method of Claim 10, wherein:

the digital value comprises a plurality of bits; and

the step of storing comprises storing the data signal in a bit of the digital value.

12. The method of Claim 10, further comprising:

increasing the current signal if the data signal indicates that the second characteristic signal is less than the first characteristic signal; and

decreasing the current signal if the data signal indicates that the second characteristic signal is greater than the first characteristic signal.

13. The method of Claim 1, further comprising tuning a filter using the stored digital value.

14. A tuning circuit, comprising:

a signal generator operable to generate a first characteristic signal;

a master circuit operable to receive a current signal and to generate a second characteristic signal in response to the current signal;

a controller operable to determine an adjustment to the current signal based at least in part upon the first and second characteristic signals; and

a memory operable to store a digital value representing the adjustment.

15. The circuit of Claim 14, wherein the controller is further operable to:

repeat the steps iteratively; and

update the digital value after each iteration.

16. The circuit of Claim 15, wherein:

the digital value comprises a plurality of bits; and

the controller is further operable to store the result of each iteration in a bit of the digital value.

17. The circuit of Claim 15, further comprising a counter operable to maintain a count of the number of iterations, wherein the controller is further operable to stop the iterative repetition of the steps in response to the count reaching a predetermined number.

18. The circuit of Claim 15, wherein the adjustment to the current value during a particular iteration is based on the last bit stored in the digital value.

19. The circuit of Claim 14, wherein the first characteristic signal comprises a voltage measured across a reference capacitor and the second characteristic signal comprises a voltage measured across a capacitor of the master circuit.

20. The circuit of Claim 19, wherein the controller determines the adjustment based on a comparison of the voltages across the respective capacitors when the external reference capacitor reaches a predetermined voltage.

21. The circuit of Claim 14, wherein:

the master circuit is part of an integrated circuit; and

the signal generator comprises:

an external reference capacitor; and

an external reference resistor.

22. The circuit of Claim 14, wherein the memory continues to store the digital value even if one or more of the signal generator, master circuit, and the controller is powered down or disabled.

23. The circuit of Claim 14, wherein:

the controller is further operable to receive a clock signal indicating that the first characteristic signal has reached a predetermined voltage; and

the controller is further operable to store a data signal in the memory in response to the clock signal, the data signal indicating whether the second characteristic signal is greater or less than the first characteristic signal.

24. The circuit of Claim 23, wherein:

the digital value comprises a plurality of bits; and

the memory is further operable to store the data signal in a bit of the digital value.

25. The circuit of Claim 23, wherein the controller is further operable to:

increase the current signal if the data signal indicates that the second characteristic signal is less than the first characteristic signal; and

decrease the current signal if the data signal indicates that the second characteristic signal is greater than the first characteristic signal.

26. The circuit of Claim 14, further comprising a filter that is tuned using the stored digital value.

27. A circuit, comprising:

a first comparator operable to:

compare a first voltage across a first capacitor to a reference voltage; and

generate a signal when the first voltage reaches the reference voltage;

a second comparator operable to compare a second voltage measured across a second capacitor to a third voltage;

a counter operable to maintain a count of the number of signals generated by the first comparator;

a memory operable to store a digital value comprising a plurality of bits; and

a controller operable to receive the signal from the first comparator and, in response, to store the result of the comparison performed by the second comparator in a particular bit of the digital value identified by the count on the counter.

28. The circuit of Claim 27, further comprising a reference current source coupled to the first capacitor and operable to charge the first capacitor.

29. The circuit of Claim 27, further comprising a variable current source coupled to the second capacitor and operable to charge the second capacitor, wherein the amount of current produced by the variable current source is adjusted based on the result of the comparison performed by the second comparator.

30. The circuit of Claim 27, wherein the value of the third voltage comprises the value of the reference voltage.

31. The circuit of Claim 27, wherein the value of the third voltage comprises the value of the first voltage.

32. The circuit of Claim 27, further comprising a filter that is tuned using the stored digital value.

33. A system, comprising:

means for generating a first characteristic signal;

means for generating a second characteristic signal in response to a current signal;

means for determining an adjustment to the current signal based at least in part upon the first and second characteristic signals; and

means for storing a digital value representing the adjustment.